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Certified Embedded Professional Multi-Core

Agenda VectorAcademy

Delivery Format:	The certification includes E-Learning content with integrated step-by-step configurations and exercises as well as remote sessions. It concludes with a final exam (theoretical & practical).
Duration:	17 weeks (~10 hours per week)
Target Group:	Project leaders, AUTOSAR ECU developers and integrators
Prerequisites:	Solid software development knowledge in AUTOSAR Classic (>2 years of practical experience) **Recommendation**: Prior participation in Certified Embedded Associate AUTOSAR Classic
Goal:	Acquire expert knowledge in the field of multi-core in Vector's MICROSAR Classic solution; Award of the certification "Certified Embedded Professional – Multi-Core"

1. Multi-Core Basics

- Motivation to use multi-core ECUs
- Overview of the multi-core use cases
- MICROSAR stack capabilities
- Design review and trace analysis with TA Tool Suite
- Optimizations for single-core environment

2. Application Split

- Features of Os and Rte for multi-core
- From single-core to multi-core configuration
- Synchronized startup and shutdown

3. BSW-Split: COM and Multi-Instance CAN

- Master BSW-split use cases (multi-instance COM and CAN)
- Deep understanding and application of PduR multi-core usage
- Ensure comprehensive multi-core integration for related modules

4. BSW-Split: Ethernet and Multi-Instance Ethernet

- Master BSW-split use cases (Ethernet and Multi-Instance Ethernet)
- Design and configure Eth stack BSW-split
- Configuration of BswM, PduR and UdpNm for seamless communication
- Deep understanding of the Ethernet-split use case

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5. **Multi-Core Crypto and Memory Stack**
   - Efficient handling of NVM blocks in multi-core environment
   - Understanding the overhead due to cross-core CS NVM ports
   - Configuration of NvSWC proxy for efficient communication
   - Achieving workload distribution by enabling crypto stack multi-core features

6. **Multi-Core WdgM and Dem Master/Satellite**
   - Learn and understand the multi-core aspects of Wdg stack
   - Configure the Wdg stack to run in multi-core environment
   - Efficient handling of Dem events with support of Master/Satellite architecture
   - Configuration of Dem Master/Satellite use case
   - Correct usage of related memory mapping to realize safety aspects

7. **Vector**
   - Communication channels to Vector

Schedule:

